Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		memory.ti. and (track$3 same (bit adj line$1) same precharg$3 same reset	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 13:46
		memory.ti. and track$3 same (bit adj line$1) same precharg$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 11:22
		"bit line pairs" same vari$5 same equal$5 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:41
		time same precharge same (voltage and temperature) same ("bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:15
		predetermined same voltage same temperature same vari$6	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:11
		predetermined same voltage same temperature same vari$	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:10
L2	2	memory.ti. and (track$3 same (bit adj line$1) same precharg$3 same reset)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 13:50
L3	1	("6,629,194").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:00
L4	0	("rowsamecolumnsamedecodersameaddress$3sameclock").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:00
L5	2628	row same column same decoder same address$3 same clock	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:01
L6	407	row same column same decoder same address$3 same "internal clock"	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:01
L7	55	row same column same decoder same address$3 same "internal clock" same "memory cells"	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:17
L8	1	("5,946,251").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:26
L9	1	("6,434,082").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 14:26
S1	30010	predetermined same voltage same temperature	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:11

S2	4723	predetermined same voltage same temperature same variations	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:11
S3	301	"predetermined time" same voltage same temperature same variations	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:11
S4	301	"predetermined time" same voltage same temperature same variations	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:13
S5	15	"predetermined time" same voltage same temperature same variations and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:15
S6	31	predetermined same precharge same voltage same temperature and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 14:21
S7	69	time same precharge same voltage same temperature and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 14:37
S8	456	(crossbar with (map$4 TLB translat$4))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 16:08
S9	32	(crossbar with (map$4 TLB translat$4)) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 16:28
S10	62	(crossbar with (map$4 TLB translat$4)) same memory and memory.ab.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 16:32
S11	114	(crossbar with (map$4 TLB translat$4)) same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/27 16:35
S12	32	(crossbar with (map$4 TLB translat$4)) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/31 12:18
S13	34	"image forming device" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/31 15:00
S14	2	("1063128").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/31 12:21
S15	0	("10663128").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/31 12:21
S16	279	"image forming" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/31 15:00
S17	35	time same precharge same voltage same temperature same "bit line" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 14:39

S18	101	time same (precharge predetermined) same (voltage temperature) same "bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 14:58
S19	1	time same (precharge and precharge) same (voltage and temperature) same "bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:00
S20	1	time same (precharge and precharge) same (voltage and temperature) same ("bit line" adj pair$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:15
S21	1	time same precharge same (voltage and temperature) same "bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:25
S22	1	precharge same (voltage and temperature) same "bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:28
S23	557	precharge same "bit line pairs" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:47
S24	99	precharge same "bit line pairs" same predetermined and memory. ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:28
S25	3319	precharge same "bit line" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:47
S26	1135	"bit line precharge" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 17:06
S27	143	"bit line precharge" same complet$4 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/01 15:48
S28	76	"bit line precharge" and precharge. ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 13:16
S29	10	"bit line precharge" same detect$3 same indicat$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 13:17
S30	213	"bit line precharge" same (detect$3 indicat$3) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 15:12
S31	24	"bit line precharge" same (detect$3 indicat$3) same transition$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:40
S32	5	"bit line precharge" same (detect$3 indicat$3) same transition$3 same clock$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:43

S33	18	"bit line precharge" same (detect$3 and indicat$3) and transition$3 and clock$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:44
S34	84	"bit line precharge" and (detect$3 same indicat$3) and transition$3 and clock$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:45
S35	5	"bit line precharge" same (transition$3 and clock$3) and (detect$3 same indicat$3) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:47
S36	1	"bit line precharge" same ready same transition$3 and (detect$3 same indicat$3) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:48
S37	18	"bit line precharge" same ready and detect$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:49
S38	5	"bit line precharge" same ready same transition and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:50
S39	5	"bit line precharge" same ready same transition	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 16:50
S40	84	"bit line precharge" same transition	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:31
S41	97	"bit line precharge" same transition$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:32
S42	20	"bit line" same precharge same transition$3 same internal same clock	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:40
S43	0	"bit line pairs" same varied same equal$5 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:41
S44	150	"bit line pairs" same (voltage temperature) same equaliz$3 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 11:36
S45	1	"complement bit line pairs" same (voltage temperature) same equaliz$3 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:48
S46	1	"bit line pairs" same variations same (voltage temperature) same equaliz$3 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:48
S47	0	"bit line pairs" same varies same (voltage temperature) same equaliz$3 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:48
S48	1	"bit line pairs" same changes same (voltage temperature) same equaliz$3 same precharg$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/02 17:48

S49	125	"bit line pairs" same (voltage temperature) same equaliz$3 same precharg$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 12:29
S50	21	"bit line pairs" same (voltage temperature) same equaliz$3 same precharg$3 same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 12:30
S51	2	"bit line precharge" same transition$3 adj3 clock same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:35
S52	1	("5754487").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 12:38
S53	2	"bit line precharge" same (transition$3 adj3 clock) same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 13:57
S54	5	"bit line precharge" same (transition$3 adj3 clock) and (row$1 same column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 13:58
S55	54	"bit line precharge" same transition$3 and (row$1 same column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 14:32
S56	1	("5,946,251").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 15:18
S57	1	("5,239,639").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 15:18
S58	1	("6,434,082").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 15:18
S59	2	"bit line precharge" same transition$3 same clock same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:36
S60	2	"bit line" adj precharge$3 same transition$3 same clock same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:36
S61	6	"bit line" adj precharge$3 same transition$3 same clock and (row$1 same column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:38
S62	61	"bit line" adj precharge$3 same transition$3 and (row$1 same column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:42
S63	39	"bit line" same precharg$3 same transition$3 same (row$1 and column$1) and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:46

S64	721	trigger$3 same transition$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:46
S65	1	(trigger$3 adj3 transition$3) same "bit line precharge" and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:47
S66	5	(trigger$3 adj3 transition$3) same "bit line" same precharg$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:47
S67	6	((trigger$3 initiat$3) adj3 transition$3) same "bit line" same precharg$3 and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 16:55
S68	15	((trigger$3 initiat$3) same transition$3) same "bit line" same precharg$3 same clock and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 17:15
S69	1	((trigger$3 initiat$3 start$3 begin$3) adj3 transition$3) same "bit line" same precharg$3 same disabl$3 same clock and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 17:16
S70	3	((trigger$3 initiat$3 start$3 begin$3) same transition$3) same "bit line" same precharg$3 same disabl$3 same clock and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/03 17:17
S71	6	transition$3 same "bit line" same precharg$3 same disabl$3 same clock and memory.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 10:52
S72	1	memory.ti. and tracking same "complementary bit lines" same differential same clock same precharge	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 10:54
S73	1	memory.ti. and tracking same "bit lines" same clock same precharge	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 10:55
S74	10	memory.ti. and (track$3 same "bit lines" same clock same precharg$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 11:04
S75	1	memory.ti. and ((track$3 adj circuit) same "bit lines" same clock same precharg$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 11:20
S76	2	memory.ti. and ((track$3 adj circuit$2) same (bit adj line$1) same precharg$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 11:22
S77	44	memory.ti. and (track$3 same (bit adj line$1) same precharg$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/04 13:46